AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-41 (Cancelled)

42. (new) A method of forming electrodes on first and second respective regions of a semiconductor structure, comprising:

a. depositing metal on a surface of a first region of the semiconductor structure;

b. forming a patterned mask over the metal on the surface of the first region, the mask having an opening so that a first portion is covered by the mask and a second portion aligned with the opening is left uncovered by the mask;

c. removing metal aligned with the opening in the second portion thereby defining a first electrode overlying and making electrical contact with the first region of the semiconductor structure;

d. removing material of the semiconductor structure aligned with the opening in the second portion to expose a surface of the second region of the semiconductor structure; and

e. forming a second electrode making electrical contact with the second region of the semiconductor structure;

43. (new) The method of claim 42, wherein the step of depositing metal comprises depositing a first metal and subsequently depositing a second metal over the first metal.

44. (new) The method of claim 43, wherein the first metal comprises nickel and the second metal comprises gold, and further comprising annealing the structure so that the metal layers form a substantially transparent material.

45. (new) The method of claim 42, wherein the step of depositing comprises electron beam deposition.

46. (new) The method of claim 42, wherein the step of forming a patterned mask comprises applying a resist on the metal to form a resist layer, and lithographically patterning the resist layer to form the at least one opening over the second region so that the remaining resist layer overlies the semiconductor structure in the first region.

47. (new) The method of claim 42, wherein the step of removing metal comprises etching.

48. (new) The method of claim 42, wherein the step of etching comprises etching with KI:I2:DI solution.

49. (new) The method of claim 46, wherein the step of removing material from the semiconductor structure comprises etching the semiconductor structure while the resist layer remains over the semiconductor structure in the first region.

50. (new) The method of claim 42, wherein the step of removing material from the semiconductor structure comprises a reactive ion etching.

51. (new) The method of claim 42, wherein the step of etching comprises etching with $BC1_3$.

52. (new) The method of claim 49, wherein the resist layer covering the first region has an edge circumscribing the opening and the step of removing metal removes some of the metal underneath the resist layer adjacent the edge of the resist layer to form a gap between the edge of the resist layer and the metal on the semiconductor structure.

53. (new) The method of claim 52, wherein the metal in the first region substantially covers the first region except in said gap.

53. (new) The method of claim 49, wherein the step of removing material from the semiconductor structure in the second region is performed so as to leave the first region protruding from the remainder of semiconductor structure.

54. (new) The method of claim 42, wherein the first region of the semiconductor structure includes a p-type semiconductor layer, and the second region includes an n-type

semiconductor layer arranged beneath the p-type semiconductor layer, the semiconductor structure having a junction between the p-type layer and the n-type layer.

55. (new) The method of claim 54, wherein, after material is removed from the semiconductor structure in the second region, and upwardly protruding portion comprising the p-type layer and a lower region comprising a portion of the n-type layer are formed.

56. (new) The method of claim 54, wherein the metal covers a large portion of the semiconductor structure in the first region, the metal being in contact with the p-type layer.

57. (new) The method of claim 54, wherein the step of forming a second electrode includes depositing metal to make electrical contact with the n-type layer of the second region.